IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	
GILBERT P. HYATT	Group Art Unit: 2189
Serial No.: 06/848,017	Examiner: Reginald Bragdon
Filed: April 3, 1986	
Docket No.: 307	
For: AN INTEGRATED CIRCUIT FILTER PROCESSOR	

TRANSMITTAL LETTER

Hon. Commissioner For Patents
P.O. Box 1450, Alexandria, VA 22313-1450

Sir:

Transmitted herewith is:

1. RESPONSE TO THE REQUIREMENT FOR INFORMATION
2. PETITION FOR EXTENSION OF TIME
3. TELEPHONE CONFERENCE RECORD
4. AMENDMENT

The fees are calculated below.

CLAIMS AS AMENDED

Claims Remaining After Amendment		Highest No. Prev. Paid For	Present Extra	Rate		Additional Fee
Total Claims	Minus	=	0	X$ 25.00	=	$ 0.00
Indep Claims	Minus	=	0	X$100.00	=	$ 0.00
Extension of Time (4-months)						$ 795.00
Total Fee						$ 795.00

Charge $ 795.00 to Deposit Account No. 08-3626.
A Declaration claiming small entity status has been filed herein.

Please charge any fees associated with the papers transmitted herewith to Deposit Account No. 08-3626, including any fees that may be required but are not set forth above. A Declaration claiming small entity status has been filed herein.

CERTIFICATION OF MAILING BY EXPRESS MAIL: I hereby certify that this correspondence is being deposited with the United States Postal Service with Express Mail post office to addressee service under 37 CFR 1.10, postage prepaid, in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 with the express mail label number EV 748457981 on September 21, 2006.

Dated: September 21, 2006

Respectfully submitted,

Gilbert P. Hyatt

Gilbert P. Hyatt
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TRANSMITTAL LETTER FOR THE TELEPHONE CONFERENCE RECORD

Hon. Commissioner For Patents
P.O. Box 1450, Alexandria, VA 22313-1450

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TELEPHONE CONFERENCE RECORD

Hon. Commissioner For Patents
P.O. Box 1450, Alexandria, VA 22313-1450

The Applicant telephoned Examiner Bragdon (who is also the supervisor (SPE)) on September 6, 2006 and requested guidance and clarification for the various Requirements For Information dated March 21, 2006 and the various Supplemental Requirements For Information dated August 25, 2006.

The Applicant explained to the Examiner that the responses to the Requirements For Information were *bona fide* because the Applicant had addressed each and every issue in a substantive manner, he had responded based upon his understanding of the wording of the stipulations and interrogatories, and a significant amount of time and work was spent in generating these responses. The Examiner explained that he had to say that the responses were not *bona fide* or he would have had to give the Applicant additional time to respond. The Applicant told the Examiner that this was not a proper reason to hold that the responses were not *bona fide*. The Examiner disagreed that this was an improper reason.

The Examiner said that he wanted simple "yes" or "no" answers to the stipulations without any qualifications. The Applicant explained to the Examiner that the stipulations as they were worded did not have simple yes or no answers and that they needed qualifications.

The Applicant explained to the Examiner that he could not merely agree or disagree with Stipulation 1 without qualification. This is because the Exhibit A's had additional information in them which was not in the "priority" pages in the specification (e.g., pages 1-3 in the example case that the Examiner was using)[1] and because of the Board's decisions regarding priority. The Examiner said that he did not want the Applicant to research the ancestor files and that he did not want to hear about the Board decisions, that he only wanted the Applicant to confirm that the "priority" pages of the specification (pages 1-3)[2] were correct. The Examiner told the Applicant that he wanted a simple statement confirming that

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[1] The example case that the Examiner was using was Docket 553; Serial No. 08/479,423.

[2] The example case that the Examiner was using was Docket 553; Serial No. 08/479,423.

the "priority" pages of the specification (pages 1-3)[3] were correct and the Examiner told the Applicant that he did not have to correct the Exhibit A's or research the ancestor files.

The Applicant explained to the Examiner that, regarding the three series 600 applications, he was relying on the December 2, 1988 effective filing date for the current claims. The Examiner said that, in these cases, it was acceptable to limit the Applicant's Stipulation 1 response to the chain of applications back to the December 2, 1988 effective filing date.

The Examiner said that he did not understand what "necessarily" means regarding the responses to Stipulations 2 and 3. The Applicant explained to the Examiner that the term "necessarily" was used to convey the fact that the different functions and elements might be used together but did not have to be used together.[4] The Applicant further explained to the Examiner that "necessarily" was also used because alternative embodiments were disclosed where one alternative embodiment might be used and another alternative embodiment might not be used or vice versa. It appeared to the Applicant that the Examiner did not understand the law on alternative embodiments, so the Applicant offered to brief this issue. The Examiner said that he knew what an alternative embodiment was and he told the Applicant that he should not brief this subject.

The Examiner explained that he knew that the individual terms in Stipulations 2 and 3 were known prior art terms and that he knew what these terms mean. The Examiner explained that it would be sufficient for the Applicant to state that these individual terms were known in the prior art to complete the response to Stipulations 2 and 3.

As an example, the Examiner discussed the relationship between a scratch pad memory and a dynamic memory. The Applicant explained to the Examiner that the scratch pad memory was disclosed in the alternatives of a static embodiment and a dynamic embodiment and that the response considered such alternative embodiments with the "necessarily" statements. The Applicant explained that Stipulations 2 and 3 did not consider alternative embodiments and thus the response had to address this issue.

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[3] The example case that the Examiner was using was Docket 553; Serial No. 08/479,423.

[4] E.g.; "A 'scratch pad memory', for example, is not necessarily an 'integrated circuit memory', is not necessarily random access, is not necessarily dynamic, and it does not necessarily store operands."

The Applicant explained to the Examiner that the Federal Circuit in *Phillips* required the PTO to first look to the disclosure (the intrinsic evidence) and then to look to the prior art (the extrinsic evidence). The Examiner said that he did not want to hear about the Federal Circuit cases.

The Examiner said that he did not understand why the Applicant read different memories and different processors on the same parts of the disclosure if they were not the same. The Applicant explained to the Examiner that this resulted from the nature of the block diagrams where a single block contained multiple functions and elements, and from the disclosure of alternative embodiments which results in the same functions or elements being implemented in different ways.

The Examiner asked the Applicant why the scratch pad memory was read on three different figures; Figs. 1, 4, and 12. The Applicant explained to the Examiner that this disclosure was a top down disclosure; that Fig. 1 was a top level block diagram showing the data processor block 12 that included the scratch pad memory, that Fig. 4 was a more detailed block diagram of the data processor showing the scratch pad memory as block 110, and that Fig. 12 was a detailed schematic and block diagram of the scratch pad memory.

The Examiner did not appear to be familiar with the disclosures in the different applications. Thus, the Applicant asked the Examiner if he had read the disclosures. The Examiner said that he had "looked through the disclosures several years ago". The Applicant explained to the Examiner that he needed to understand the disclosures in order to understand the responses. The Applicant also explained to the Examiner that he needed to understand the prior art in order to understand the responses. The Applicant explained that the individual terms involved in Stipulations 2 and 3 were know prior art terms, that just the differences in the names show that there are differences between the terms, and that many of these terms are compatible with each other. The Examiner asked about the specific example of a dynamic memory and a scratch pad memory and the Applicant again explained that the scratch pad memory was disclosed as the alternatives of a static implementation and a dynamic implementation.

Regarding the amendments to the claims, the Applicant explained to the Examiner that an amendment to the claims that recited all of the unamended claims would require more than 100 pages in the example case that the Examiner was using[5] and, for economy of paper, the short form claim amendments were used. The Examiner said that it would be sufficient for the Applicant to state that he intended to amend these claims in the next full amendment. The Applicant told the Examiner that he would follow this advice. The Examiner said that he would check into the alternative of entering an examiner's amendment and that the Applicant should authorized the Examiner to make such an Examiner's amendment for those short form amendments. The Applicant hereby authorizes the Examiner to make an Examiner's amendment for these short form claims.

Respectfully submitted,

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[5] The example case that the Examiner was using was Docket 553; Serial No. 08/479,423.

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RESPONSE TO REQUIREMENT FOR INFORMATION UNDER 37 C.F.R. § 1.105

Hon. Commissioner For Patents
P.O. Box 1450, Alexandria, VA 22313-1450

I. OVERVIEW

This Response is provided in response to a Requirement For Information under 37 C.F.R. § 1.105 dated March 21, 2006 (herein the "105 Requirement"). This Response is also in response to the guidance and clarification given by the Examiner in a telephone conference with the Applicant. *See* the Telephone Conference Record transmitted herewith.

The Initial 105 Requirement required a response to Stipulations and to Interrogatories having numerous numbered parts. This is a good faith Response that substantively addresses each and every one of the requirements.

The Applicant herein provides a response to Stipulations 1-3 and the Interrogatories and objects to Stipulations 1-3 and the Interrogatories in the 105 Requirement.

II. RESPONSE TO THE EXAMINER'S STIPULATION 1

In the Stipulation 1 the Applicant is required to agree or disagree with the following:

> 1. Attached "Exhibit A" is a correct representation of Applicant's claim for priority under 35 U.S.C. § 120 based on Applicant's statements on pages 37-40 of the amendment received 30 July 1990.

The Applicant responds by stating that: the Applicant disagrees.

However, Exhibit A appears to be "a correct representation of Applicants claim for priority ....". However, the applicant does not have ready access to all of the file histories of the ancestor applications. Thus he is unable to confirm the representation. Further, in full compliance with the Examiner's requirement (*see* the Telephone Conference Record) the Applicant has not researched "the file histories of the ancestor applications."

The Applicant makes note that the Board in the decisions in the following appeals has made specific findings regarding the effective filing dates of claimed subject matter and of the continuation in part status of certain applications:

1. Docket No. 555; Appeal No. 2003-0794
2. Docket No. 556; Appeal No. 2002-0495
3. Docket No. 558; Appeal No. 2002-0626
4. Docket No. 563; Appeal No. 2004-2333
5. Docket No. 565; Appeal No. 2001-2171
6. Docket No. 566; Appeal No. 2002-2032

See the copies of the decisions in these appeals transmitted with the papers in application Serial No. 08/471,931 dated July 21, 2006 and incorporated herein by reference (the Related Proceedings Appendix).

Further, the following stipulation is made in view of the telephone conference with the Examiner:

> The Applicant stipulates that the "Applicant's claim to priority on pages 37-40 of the present specification ...." is correct except as modified by the determinations of the Board.

However, Stipulation 1 is ambiguous and the Applicant therefore further responds in an effort to provide a full, good faith response. To the extent that Stipulation 1 requires a comparison of Exhibit A to the Applicant's claim for priority, there are significant variances between the two.

The Applicant is currently relying on the February 14, 1975 effective filing data of ancestor application SN05/550,232 for the instant claims. Priority is obtained from the chain of copendency of the instant application with the following patent applications: 06/160,872 and 06/425,731. This priority is obtained from the copendency of the '023 application with the ''872 applicaton, the '872 application with the '731 application, which was copending with the instant application. However, in full compliance with the Examiner's requirement (*see* the Telephone Conference Record) the applicant has not researched "the file histories of the ancestor applications.

Exhibit A omits the title and inventor designations that are provided in the claim for priority. Exhibit A provides patent numbers and issue dates that are not found in the claim for priority. Exhibit A also adds application series numbers, *e.g.*, "07/", to the patent application numbers in the claim for priority

III. RESPONSE TO THE EXAMINER'S STIPULATON 2

The Examiner has given conflicting guidance and clarification in the telephone conference. As a result, it is not clear as to what should be the proper response to Stipulation 2. Nevertheless, the Applicant will respond based upon his reasonable understanding of Stipulation 2.

The Stipulation 2 states:

> 2. The terminology "alterable memory" (e.g. claim 102), "random access memory" (e.g. claim 5), and "operand memory" (e.g. claim 104) as used throughout the claims refers to the same memory and are in fact just different labels with no patentable distinctions and therefor are equivalent structures.

In the telephone conference on September 6, 2006 the Examiner stated that he would accept as a sufficient response a statement that each of the individual terms in the stipulation were known in the prior art. Applicant thus acknowledges that each of the following terms were known in the prior art.

"alterable memory"

"random access memory"

"operand memory"

The Applicant further responds by stating that he disagrees with Stipulation 2.

The Applicant contends that the differences in the terms, which are inherent in the terms themselves, are as follows:

a. "alterable memory" v. "random access memory"

An alterable memory might or might not be a random access memory.

A random access memory might or might not be an alterable memory.

b. "alterable memory" v. "operand memory"

An alterable memory might or might not be an operand memory.

An operand memory might or might not be an alterable memory.

c. "random access memory" v. "operand memory"

A random access memory might or might not be an operand memory.

An operand memory might or might not be a random access memory.

Following Stipulation 2 the Requirement states, "Applicant is required to point out the differences between the terms (if any) and how these differences are supported in the specification, or the prior art at the time the invention was made."

The Applicant has pointed out the differences between the terms above. Further, the differences are shown by the terms themselves.

Stipulation 2 further requires the Applicant to point out how these "differences" are "supported" in the specification, or the prior art at the time the invention was made.

The Applicant objects to this requirement as being compound, calling for a legal opinion, ambiguous, indefinite and unintelligible. Different kinds of memories or computers are different and the differences are what they are. The different names convey the differences. In the telephone conference, the Examiner stated that he knew what these terms mean. Thus, the Applicant should not be burdened with stipulations about terms that are known in the art and that are known by the Examiner. After all, these are not abstract terms dreamed up in an obscure art,

they are electronic terms that have been known for more than 35 years and are known by the Examiner. The Applicant has pointed out these differences above.

Further, the Applicant does not understand how the differences can be "supported" by either the specification or the prior art. The word "supported" has not been defined and the Applicant does not know what it means to support differences in this context. A disclosure is not focused on supporting differences, it is focused on enablement and written description.

Notwithstanding the unintelligibility of the phrase, the Applicant has attached Exhibit B to this response to show where the various terms are used in the disclosure. herein. The Applicant excerpted and cited to the disclosure regarding the use of the terms. However, pointing out differences between functions or elements is not known to be an objective of a patent disclosure.

The requirement to point out how these "differences" are "supported" by the prior art at the time the invention was made is in violation of 37 C.F.R. 1.105 in that it is a burden on the Applicant and it would require a search of the distant prior art. *See* the sections below regarding the Applicant's objections. Further, this information is not readily available to the Applicant. Such a response is to be accepted as a complete reply under 37 C.F.R. § 1.105(a)(4).

Despite the ambiguousness, indefiniteness and unintelligibility of this Stipulation the Applicant has made a *bona fide* response.

IV. RESPONSE TO THE EXAMINER'S STIPULATON 3

The Examiner has given conflicting guidance and clarification in the telephone conference. As a result, it is not clear as to what should be the proper response to Stipulation 3. Nevertheless, the Applicant will respond based upon his reasonable understanding of Stipulation 3.

The Stipulation 3 states:

> 3. The terminology "integrated circuit digital signal processor" (e.g. claim 42), "single integrated circuit chip having a digital signal processor" (e.g. claim 53), and "monolithic integrated circuit data processor" (e.g. claim 164) as used throughout the claims refers to the same "single-chip" processor and are in fact just different labels with no patentable distinctions and therefor are equivalent structures.

In the telephone conference on September 6, 2006 the Examiner stated that he would accept as a sufficient response a statement that each of the individual terms in the stipulation were known in the prior art. Applicant thus acknowledges that each of the following terms were known in the prior art.

"integrated circuit"

"digital signal processor"

"single integrated circuit chip"

"monolithic integrated circuit"

"data processor"

The Applicant further responds by stating that he disagrees with Stipulation 3.

The Applicant contends that the differences in the terms, which are inherent in the terms themselves, are as follows:

a. "integrated circuit digital signal processor" v. "single integrated circuit chip having a digital signal processor"

As far as the Applicant is aware an integrated circuit digital signal processor is not a single integrated circuit chip having a digital signal processor.

As far as the Applicant is aware a single integrated circuit chip having a digital signal processor is not an integrated circuit digital signal processor.

b. "integrated circuit digital signal processor" v. "monolithic integrated circuit data processor"

An integrated circuit digital signal processor may or may not be a monolithic integrated circuit data processor.

A monolithic integrated circuit data processor may or may not be an integrated circuit digital signal processor.

c. "single integrated circuit chip having a digital signal processor" v. "monolithic integrated circuit data processor"

As far as the Applicant is aware a single integrated circuit chip having a digital signal processor is not a monolithic integrated circuit data processor.

As far as the Applicant is aware a monolithic integrated circuit data processor is not a single integrated circuit chip having a digital signal processor.

Following Stipulation 3 the Requirement states, "Applicant is required to point out the differences between the terms (if any) and how these differences are supported in the specification, or the prior art at the time the invention was made."

The Applicant has pointed out the differences between the terms above. Further, the differences are shown by the terms themselves.

Stipulation 3 further requires the Applicant to point out how these "differences" are "supported" in the specification, or the prior art at the time the invention was made.

The Applicant objects to this requirement as being compound, calling for a legal opinion, ambiguous, indefinite and unintelligible. Different kinds of memories or computers are different and the differences are what they are. The different names convey the differences. In the telephone conference, the Examiner stated that he knew what these terms mean. Thus, the Applicant should not be burdened with stipulations about terms that are known in the art and that are known by the Examiner. After all, these are not abstract terms dreamed up in an obscure art, they are electronic terms that have been known for more than 35 years and are known by the Examiner. The Applicant has pointed out these differences above.

Further, the Applicant does not understand how the differences can be "supported" by either the specification or the prior art. The word "supported" has not been defined and the Applicant does not know what it means to support differences in this context. A disclosure is not focused on supporting differences, it is focused on enablement and written description.

Notwithstanding the unintelligibility of the phrase, the Applicant has attached Exhibit B2 to this response to show where the various terms are used in the disclosure. herein. The Applicant excerpted and cited to the disclosure regarding the use of the terms. However, pointing out differences between functions or elements is not known to be an objective of a patent disclosure. The requirement to point out how these "differences" are "supported" by the prior art at the time the invention was made is in violation of 37 C.F.R. 1.105 in that it is a burden on the Applicant and it would require a search of the distant prior art. *See* the sections befow regarding the Applicant's objections. Further, this information is not readily available to the Applicant. Such a response is to be accepted as a complete reply under 37 C.F.R. § 1.105(a)(4).

Despite the ambiguousness, indefiniteness and unintelligibility of this Stipulation the Applicant has made a *bona fide* response.

V. RESPONSE TO THE EXAMINER'S INTERROGATORIES

Representative support in the disclosures for the statements set forth in the Interrogatories is provided in Exhibit C attached hereto. The citations to the disclosure and the excerpts from the disclosure in Exhibit B and in Exhibit C of the instant Response are the same in pertinent part in the instant disclosure and in the disclosures in applications SN05/550,232; 06/160,872; and 06/425,731. However, in full compliance with the Examiner's requirement (*see* the Telephone Conference Record) the Applicant has not researched "the file histories of the ancestor applications.

VI. THE APPLICANT OBJECTS TO STIPULATION 1

The 105 Requirement is ambiguous and misleading and does not request the information sought by the Examiner. *See* the objections stated herein. Even the Examiner recognized the impropriety of the Stipulation implicit in the changes made to the Stipulation in the telephone conference In the telephone conference the Examiner stated that he wanted the Applicant to confirm that the Applicant's claim for priority was correct but that Applicant need not consult ancestor file histories and the Applicant has complied. However, this requirement is much different than what is stated in Stipulation 1 and thus it points out the ambiguity of Stipulation 1. In view of this ambiguity, the Applicant requests that Stipulation 1 be withdrawn.

VII. THE APPLICANT OBJECTS TO STIPULATION 2

The Applicant objects to Stipulation 2 as being hopelessly compound, calling for a legal opinion and being ambiguous, indefinite and unintelligible. Stipulation 2 lists several terms which are the same in some implementations and different in other implementations. Yet Stipulation 2 demands a single unqualified answer as to (1) whether the terms as used throughout the claims refer to the same memory, (2) whether the terms are in fact just different labels, (3) whether the terms have no patentable distinctions, and (4) whether the terms therefore are equivalent structures (the "four qualifiers"). A single "agree" or "disagree" answer was demanded even though there are many combinations of different answers as each different pair of terms is applied to each of these four qualifiers at the end of the request.

The requirement to consider the terms "as used throughout the claims" is indefinite since the terms may be used differently in different claims. Without reference to the way a specific term is used in a specific claim there can be no meaningful response to the stipulation. Further, the comparisons have no single "agree" or "disagree" answer. For example, the first two terms were "alterable memory" and "random access memory". Some alterable memories are random access memories while others are not. The same applies to most of the other pairs of terms. There is no single "agree" or "disagree" answer even though such was demanded.

Stipulation 2 demands to know in a single "agree" or "disagree" answer whether there are patentable distinctions between the terms. However, patentable distinctions must be determined in the context of each claim as a whole and in the context of the prior art and cannot be determined by looking at pairs of terms in isolation. Furthermore, whether or not there are patentable distinctions calls for a legal opinion that is not the proper subject matter for a 37 C.F.R. 1.105. *See* the discussion herein regarding the impropriety of seeking opinions in a 37 C.F.R. 1.105 Requirement.

Stipulation 2 also demands to know whether all of the terms are equivalent structures. This demand is indefinite, unintelligible and calls for a legal opinion. There is no definition of what "equivalent" is supposed to mean or what "structure" is supposed to mean. In the sense that all of the terms refer to memories that store data and without definitions, they may be considered to have somewhat equivalent structures on a very general level. In the sense that memories were implemented in different ways and performed different functions (e.g., static storage or dynamic storage, random access or sequential access, and integrated circuit construction or discrete component construction), they may be considered to have different structures. Thus, they all have potentially different structures and, on a very general level, may have potentially the same structures. For example, an alterable memory might or might not be an integrated circuit memory. The Applicant does not know what test to apply to determine if they are "equivalent structures". The term could refer to the doctrine of **equivalents** for determining infringement. Such a determination must be made on a claim by claim basis and involves a legal opinion that requires a given infringement context. It cannot be made in the abstract. Such an opinion is inappropriate under 37 C.F.R. 1.105 in the present context. *See* the discussion herein regarding the impropriety of seeking opinions in a 37 C.F.R. 1.105 Requirement.

The Applicant is required to "ascertain whether there are any differences of any significance among these terms and how such differences are to be attributed". The Applicant is required to point out the differences between the terms (if any) and how these differences are supported in the specification, or the prior art at the time the invention was made."

The requirement is indefinite since not even a hint provided as to what constitutes a significant difference. As pointed out, most of the terms might have differences and might have similarities. All have similarities in that they are memories. The Applicant responded in a

reasonable manner considering that the Stipulation does not define what constitutes a significant difference between various memories. .

The Applicant was further required to point out how the differences are "supported in the specification, or in the prior art." Again, not a hint is provided as to what is meant by supporting a difference. This requirement is unintelligible. Further, there is no basis for the assumption that the differences are in fact supported in either the disclosure or the prior art, much less in a reasonable way that can be determined without excessive burden, yet the Applicant is required on pain of abandoning his patent application to show where this support is to be found. The Applicant has attempted to show this support by attaching Exhibit B to show how the terms are used in the disclosure. Because Stipulation 2 is hopelessly compound, calls for a legal opinion, and is ambiguous, indefinite, and unintelligible, it should therefore be withdrawn.

VIII. THE APPLICANT OBJECTS TO STIPULATION 3

The Applicant objects to Stipulation 3 as being hopelessly compound, calling for a legal opinion and being ambiguous, indefinite and unintelligible. Stipulation 3 lists several terms which are the same in some implementations and different in other implementations. Yet Stipulation 3 demands a single unqualified answer as to (1) whether the terms as used throughout the claims refer to the same memory, (2) whether the terms are in fact just different labels, (3) whether the terms have no patentable distinctions, and (4) whether the terms therefore are equivalent structures (the "four qualifiers"). A single "agree" or "disagree" answer was demanded even though there are many combinations of different answers as each different pair of terms is applied to each of these four qualifiers at the end of the request.

The requirement to consider the terms "as used throughout the claims" is indefinite since the terms may be used differently in different claims. Without reference to the way a specific term is used in a specific claim there can be no meaningful response to the stipulation. Further, the comparisons have no single "agree" or "disagree" answer. For example, the first two terms were "integrated circuit digital signal processor" and "single integrated circuit chip having a digital signal processor". Some alterable integrated circuit digital signal processors are single integrated circuit chip digital signal processor while others are not. A digital signal processor is not a single integrated circuit chip, whether or not the chip has a digital signal processor. The same applies to most of the other pairs of terms. There is no single "agree" or "disagree" answer even though such was demanded.

Stipulation 3 demands to know in a single "agree" or "disagree" answer whether there are patentable distinctions between the terms. However, patentable distinctions must be determined in the context of each claim as a whole and in the context of the prior art and cannot be

determined by looking at pairs of terms in isolation. Furthermore, whether or not there are patentable distinctions calls for a legal opinion that is not the proper subject matter for a 37 C.F.R. 1.105. *See* the discussion herein regarding the impropriety of seeking opinions in a 37 C.F.R. 1.105 Requirement.

Stipulation 3 also demands to know whether all of the terms are equivalent structures. This demand is indefinite, unintelligible and calls for a legal opinion. There is no definition of what "equivalent" is supposed to mean or what "structure" is supposed to mean. In the sense that all of the terms refer to processors and without definitions, they may be considered to have somewhat equivalent structures on a very general level. In the sense that processors were implemented in different ways and performed different functions they may be considered to have different structures. Thus, they all have potentially different structures and, on a very general level, may have potentially the same structures. The Applicant does not know what test to apply to determine if they are "equivalent structures". The term could refer to the doctrine of **equivalents** for determining infringement. Such a determination must be made on a claim by claim basis and involves a legal opinion that requires a given infringement context. It cannot be made in the abstract. Such an opinion is inappropriate under 37 C.F.R. 1.105 in the present context. *See* the discussion herein regarding the impropriety of seeking opinions in a 37 C.F.R. 1.105 Requirement.

The Applicant is required to "ascertain whether there are any differences of any significance among these terms and how such differences are to be attributed". The Applicant is required to point out the differences between the terms (if any) and how these differences are supported in the specification, or the prior art at the time the invention was made."

The requirement is indefinite since not even a hint provided as to what constitutes a significant difference. As pointed out, most of the terms might have differences and might have similarities. All have similarities in that they are processors. The Applicant responded in a reasonable manner considering that the Stipulation does not define what constitutes a significant difference between various processors.

The Applicant was further required to point out how the differences are "supported in the specification, or in the prior art." Again, not a hint is provided as to what is meant by supporting a difference. This requirement is unintelligible. Further, there is no basis for the assumption that the differences are in fact supported in either the disclosure or the prior art, much less in a reasonable way that can be determined without excessive burden, yet the Applicant is required on pain of abandoning his patent application to show where this support is to be found. The Applicant has attempted to show this support by attaching Exhibit B2 to show how the terms are used in the disclosure. Because Stipulation 3 is hopelessly compound, calls for a legal opinion, and is ambiguous, indefinite, and unintelligible, it should therefore be withdrawn.

IX. AMENDMENT

In a telephone interview with the Examiner, the Examiner stated that he would accept Amendments if the Applicant would state that he intended to amend these claims in the next full amendment. The Applicant hereby states that it is his intent to amend these claims in the next full amendment. In that telephone interview, the Examiner suggested that the Applicant authorize the Examiner to make an Examiner's amendment for these claims. The Applicant hereby authorizes the Examiner to make an Examiner's amendment for these claims.

X. THIS REQUIREMENT FOR INFORMATION IS PART OF A PATTERN OF SUCH REQUIREMENTS, WHICH IS INAPPROPRIATE

This Requirement For Information is part of a pattern of such requirements, which is inappropriate. This Requirement For Information is being misused (Federal Register Vol. 69, No. 182, page 56513, col. 1 (emphasis added)):

> Requirements for information are **not** routinely made. They are to be used only where there is an absence of necessary information within the record. Any such requirement should be tailored to treat specific issues on a case-by-case basis.

However, this and other Requirements For Information are being "routinely made" in various ones of the Applicant's copending applications, the requirements are not being made "on a case-by-case basis". For example, such Requirements For Information have been made in 26 of the Applicant's applications within the same art group (Group 2100) within a six week period. This violates the fundamental basis of 37 CFR 1.105 and the PTO's commitments to the public.

XI. OBJECTIONS TO THE 37 CFR 1.105 REQUIREMENT FOR INFORMATION

The Applicant objects to the instant Requirement for Information because it violates the policies and procedures of the PTO. For example; it violates MPEP 704.11, 704.11(b), and 704.14 and it violates the Federal Register – Rules and Regulations that relate to the instant Requirement For Information; as discussed below. Examples are provided below.

1. The PTO requires that a Requirement For Information be "focused", "specific", "concise", and "limited [in] scope". See MPEP 704.11 and see the Federal Register, Vol. 69, No. 182, pages 56511 et seq. However, the instant Requirement For Information is neither "focused", nor "specific", nor "concise", nor "limited [in] scope".
2. The PTO prohibits a Requirement For Information from placing an "undue burden" on the Applicant. See MPEP 204.11 and see the Federal Register, Vol. 69, No. 182, pages 56511 et seq. However, the broad nature of the instant Requirement For Information improperly places the prohibited "undue burden" on the Applicant.
3. The PTO prohibits a Requirement For Information from seeking an applicant's "opinion". See the Federal Register, Vol. 69, No. 182, pages 56511 et seq. However, the instant Requirement For Information improperly seeks the Applicant's "opinion".

The Applicant further objects to the instant Requirement For Information because it violates MPEP 704.11. In particular; "the scope of the requirement" has not been "narrowly defined" nor "narrowly specified and limited in scope" and the Examiner does not have "a reasonable basis for requiring [the] information" and thus, "[I]t is a significant burden on both the applicant and the Office". *See* MPEP 704.11:

> **704 What Information May Be Required ...**
>
> There must be a reasonable basis for the information required that would aid in the examination of an application or treatment of some matter. A requirement for information under 37 CFR 1.105 places a substantial burden on the applicant that is to be minimized by clearly focusing the reason for the requirement and the scope of the expected response. Thus, the scope of the requirement should be narrowly defined, and a requirement under 37 CFR 1.105 may only be made when the examiner has a reasonable basis for requiring information.

INFORMATION REASONABLY NECESSARY FOR FINDING PRIOR ART

> The criteria stated in 37 CFR 1.105 for making a requirement for information is that the information be reasonably necessary in the examination or treatment of a matter in an application. The information required would typically be that necessary for finding prior art or for resolving an issue arising from the results of the search for art or from analysis of the application file. A requirement for information necessary for finding prior art is not a substitute for the examiner performing a search of the relevant prior art; the examiner must make a search of the art according to MPEP § 704.01 and §§ 904 – 904.03.
>
> The criteria of reasonable necessity is generally met, e.g., where: ...

The statement then goes on to give two examples where "the claimed subject matter cannot be adequately searched" or where there is a "lack of relevant prior art found in the examiner's search"; neither of which are the situation in the instant case.

Further, the information sought in the Requirement is not "reasonably necessary" nor "narrowly defined", it is a substantial effort that is not focused on the instant claim limitations. *See also* MPEP 704.11, 704.14:

> **704.14 Making a Requirement for Information**
>
> A requirement for information under 37 CFR 1.105 should be narrowly specified and limited in scope. It is a significant burden on both the applicant and the Office since the applicant must collect and submit the required information and the examiner must consider all the information that is submitted. A requirement for information is only warranted where the benefit from the information exceeds the burden in obtaining information.

In particular; "the scope of the requirement" has not been "narrowly defined" nor "narrowly specified and limited in scope", the Examiner does not have "a reasonable basis for requiring [the] information", and "[I]t is a significant burden on both the applicant and the Office".

The PTO prohibits a Requirement For Information from seeking an Applicant's "opinion". *See* the Federal Register Vol. 69, No. 182, page 56512, cols. 1-2 (emphasis added):

> The terms "factual" and "facts" are included in the rule to make it clear that it is facts, and factual information, that are known to applicant, or readily obtained after reasonable inquiry by applicant, that are being sought, and that requirements under §

> 1.105(3)(3) **are not requesting opinions** that may be held or would be required to be formulated by applicant.... Applicant need not, however, derive or independently discover a fact ... in response to a requirement for information.

See also the Federal Register Vol. 69, No. 182, page 56513, col. 3:

> *Response[To Comment 67]:* To the extent that such comments are directed toward the elucidation of opinions and legal conclusions, the comments are adopted and the rule has been amended to remove the term "opinion".

See also Federal Register Vol. 69, No. 182, page 56514, col. 1 (emphasis added):

> *Response[To Comment 72]:* The comment is adopted to the extent that interrogatories and stipulations **should not be used to ask for opinions**, and that examiners will receive training in the drafting of **concise**, **focused** interrogatories and stipulations.

See also Federal Register Vol. 69, No. 182, page 56514, col. 3 (emphasis added):

> *Comment 77:* Several comments suggested that the proposed amendment to § 1.105 would be particularly onerous on *pro se* inventors.
>
> *Response[To Comment 77]:* The comment has been adopted to the extent that the comments were directed towards requiring submission of opinion evidence, *e.g.*, the level of ordinary skill in the art. Thus, this final rule making clarifies that **"opinion evidence" shall not be encouraged to be sought by a § 1.105 requirement**.

However, the instant Requirement For Information improperly seeks the Applicant's "opinion" and is far from "concise" and "focused". *See also* Federal Register Vol. 69, No. 182, page 56514, col. 1 (emphasis added):

> *Response [To Comment 72]:* The comment is adopted to the extent that interrogatories and stipulations **should not be used to ask for opinions**, and that examiners will receive training in the drafting of **concise**, **focused** interrogatories and stipulations.

CERTIFICATION OF MAILING BY EXPRESS MAIL: I hereby certify that this correspondence is being deposited with the United States Postal Service with Express Mail post office to addressee service under 37 CFR 1.10, postage prepaid, in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 with the express mail label number EV 748457981 on |September 21, 2006.

Dated: September 21, 2006

Respectfully submitted,

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EXHIBIT B

B1. The terminology "alterable memory"[1] (e.g. claim 102), "random access memory"[2] (e.g claim 5), and "operand memory"[3] (e.g. claim 104) as used throughout the claims refers to the same memory and are in fact just different labels with no patentable distinctions and therefor are equivalent structures.

. Factored Data Processing System For Dedicated Applications Ser. No. 101,881 filed on Dec. 6 *See* instant disclosure 2:35-2 (emphasis added).

"The data processor 12 is shown by way of this example to be used in conjunction with a **core memory 30**.[1] The basic architecture of this data processor will permit an integrated circuit memory, such as a read-only memory (ROM), or a random-access memory (RAM) [2]or flip-flop type memory to be substituted for the core memory 30 to provide a completely integrated circuit computer which might be called a monolithic computer." See '881 disclosure page 10:13-19 (emphasis added). See also, e.g.; '881 disclosure at Fig. 1 at 12.

"40. An electronic data processing system including read only memory means, alterable memory means and program means, said system being implemented on a single integrated circuit chip." See '881 Original Claim #40 disclosure page 111.

[3]A scratch pad memory (SPM) 110 provides storage for intermediate computational results, return addresses, indexes and other pertinent information. The SPM 110 provides rapid internal storage without the need for transferring data to the core memory. It is a group of 32 16 bit serial in, serial out registers which are divided into two pages with 16 registers on each page. *See* '881 disclosure page 36:2-8 (emphasis added). *See* also, e.g.; '881 disclosure at also Fig. 1 at 12, Fig. 4 at 110, and 12

B2. The terminology "integrated circuit digital signal processor" (e.g. claim 42), "single integrated circuit chip having a digital signal processor" (e.g. claim 53), and "monolithic integrated circuit data processor" (e.g. claim 164) as used throughout the claims refers to the same "single-chip" processor and are in fact just different labels with no patentable distinctions and therefor are equivalent structures.

. Factored Data Processing System For Dedicated Applications Ser. No. 101,881 filed on Dec. 6 *See* instant disclosure 2:35-2 (emphasis added).

"The data processor 12 is shown by way of this example to be used in conjunction with a **core memory 30.** The basic architecture of this data processor will permit an integrated circuit memory, such as a read-only memory (ROM), or a random-access memory (RAM) or flip-flop type memory to be substituted for the core memory 30 to provide a completely integrated circuit computer which might be called a monolithic computer." See '881 disclosure page 10:13-19 (emphasis added). See also, e.g.; '881 disclosure at Fig. 1 at 12.

"40. An electronic data processing system including read only memory means, alterable memory means and program means, said system being implemented on a single integrated circuit chip." See '881 Original Claim #40 disclosure page 111.

EXHIBIT C

RESPONSE TO REQUIREMENT FOR INFORMATION ITEMS 1 TO 54

1. "generating pattern recognition information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information" (e.g. claim 46). *See* e.g,

> The present invention provides signal processing and digital filtering arrangements for signal enhancement which are applicable to multitudes of different types of systems. In a geophysical exploration system, an improved digital filtering arrangement is provided which yields improved digital filtering capability with a significant reduction in cost when compared to priorart systems. Further, the availability of the low cost and high performance correlator of the present invention permits use of correlation digital filtersin multitudes of applications that previously could not qualify such digital filtering capability. For example, use of digital filters may significantly enhance processing such as in the medical diagnostic systems, equipment diagonstic systems, radar and sonar signal processing systems, patternre cognition systems, communication systems, and in many other signal processing and data processing applications." *See* instant disclosure 4:3-15 (emphasis added). *See* also, e.g.; instant disclosure at Fig. 1

2. "an amplifier coupled to the antenna and generating amplified information in response to the antenna information" (e.g. claim 47) *See* e.g.:

> Signal processor 112 may be any well known signal processor including arrangements of filters and amplifiers for processing analog signals and analog-to-digital converters (ADCs) such as used in geophysical exploration systems and acoustic imaging systems. Processed signals 113 may be digital signals from an ADC included in signal processors 112 for processing with digital devices such as compositor 114 and correlator 116. ." *See* instant disclosure 61:21-27 (emphasis added). *See* also, e.g.; instant disclosure at Fig. 1-112

> Array 110 may be an array of geophones in a geophysical application, an array of hydrophones in a sonar application, an array of radar receivers such as in a phased array antenna for radar systems, or other well known transducer arrays. *See* instant disclosure 61:9-11 (emphasis added). *See* also, e.g.; instant disclosure at Fig. 1-112

3. "generating data compressed information with an integrated circuit digital signal processor in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information." (e.g. claim 48). *See* e.g.:

> A correlator may be considered to be a device for data compression, wherein large amounts of data may be processed to compress the data into a

reduced form. *See* instant disclosure 46:1-3 (emphasis added). *See* also, e.g.; instant disclosure at Fig. 1A:116

Signal processor 112 may be any well known signal processor including arrangements of filters and amplifiers for processing analog signals and analog-to-digital converters (ADCs) such as used in geophysical exploration systems and acoustic imaging systems. Processed signals 113 may be digital signals from an ADC included in signal processors 112 for processing with digital devices such as compositor 114 and correlator 116. . *See* instant disclosure 61:21-27 (emphasis added). *See* also, e.g.; instant disclosure at Fig. 1A:112

Further, outer loop 501 is used to control sampling in the temporal-domain. Therefore, each iteration through outer loop 501 selects the next sequential sampling time t[S]; each iteration through middle loop 502 selects a sample from each of the trace signal channels N for the sample time interval controlled with outer loop 501; and each iteration through inner loop 503 selects a pilot signal sample for processing the trace signal sample that was selected with middle loop 502 for the time interval samples selected with outer loop 501. . *See* instant disclosure 107:3-10 (emphasis added). *See* also, e.g.; instant disclosure at Fig. 5-501,502,503

4. "generating iteratively processed information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information" (e.g. claim 57). *See* e.g.:

Further, outer loop 501 is used to control sampling in the temporal-domain. Therefore, each iteration through outer loop 501 selects the next sequential sampling time t[S]; each iteration through middle loop 502 selects a sample from each of the trace signal channels N for the sample time interval controlled with outer loop 501; and each iteration through inner loop 503 selects a pilot signal sample for processing the trace signal sample that was selected with middle loop 502 for the time interval samples selected with outer loop 501. . *See* instant disclosure 107:3-10 (emphasis added). *See* also, e.g.; instant disclosure at Fig. 5-501,502,503

Signal processor 112 may be any well known signal processor including arrangements of filters and amplifiers for processing analog signals and analog-to-digital converters (ADCs) such as used in geophysical exploration systems and acoustic imaging systems. Processed signals 113 may be digital signals from an ADC included in signal processors 112 for processing with digital devices such as compositor 114 and correlator 116. . *See* instant disclosure 61:21-27 (emphasis added). *See* also, e.g.; instant disclosure at Fig. 1A:112

5. "filter processor" (e.g. claim 59). *See* e.g.:

> One feature of the present invention provides high resolution output data in response to low resolution input data and low resolution computations for a digital filter processor. . *See* instant disclosure 49:1-3 (emphasis added). *See* also, e.g.; instant disclosure at Fig. 1A:112

6. "correlator filter processor" (e.g. claim 60). *See* e.g.:

> One feature of the present invention provides a real-time time-domain correlator that can accommodate the geophysical application described in the above example, including a trace signal having 32,000-samples, a pilot signal having 24,000-samples, and 1,000-channels. . *See* instant disclosure 22:26-30 (emphasis added). *See* also, e.g.; instant disclosure at Fig. 1E:104

7. "an integrated circuit multiplier circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating correlation product operands by multiplying operands in response to the instructions and an integrated circuit adder circuit coupled to the integrated circuit read only memory and to the integrated circuit multiplier circuit and generating correlation filtered operands by adding the product operands in response to the instructions" (e.g. claim 60). *See* e.g.:

> Yet another advantage may be elimination of a compositor, where compositing is a summation operation and wherein the correlation algorithm of the present invention provides multiplication and summing operations; where compositing may be implicit in the correlation operation and need not be implemented in a special compositor. . *See* instant disclosure 5:1-5 (emphasis added).
>
> Memory devices such as P-store 610 and Z-store 614 may be implemented with a read only memory (ROM) for P-store 610 and with a random access memory (RAM) for Z-store 614 to exemplify use of these different memories devices, as will be discussed in detail with reference to FIG. 6D *See* instant disclosure 139:16-19 (emphasis added). *See* also, e.g.; instant disclosure at Fig. 6D-610
>
> One feature of the present invention provides a real-time time-domain correlator that can accommodate the geophysical application described in the above example, including a trace signal having 32,000-samples, a pilot

signal having 24,000-samples, and 1,000-channels. . *See* instant disclosure 22:26-30 (emphasis added). *See* also, e.g.; instant disclosure at Fig. 1E:104

8. "generating searched information hi response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information" (e.g. claim 61). *See* e.g.:

> A correlation algorithm may be described as searching a trace signal in the temporal-domain or phase-domain to find a match with a pilot signal, wherein the correlation computation is extremely sensitive to phase considerations and may have only a secondary sensitivity to amplitude considerations. *See* instant disclosure 55:15-18 (emphasis added).
>
> A flow diagram is provided in FIG. 5A illustrating the operation of a correlation algorithm in accordance with the present invention. This algorithm may be implemented in a software form with a general purpose digital computer or in a hardwired logic form with a special purpose logical arrangement. For simplicity of discussion, the implementation of the flow diagram set forth in FIG. 5A will be exemplified with a software embodiment using a stored program computer. *See* instant disclosure 105:1-7 (emphasis added). *See* also, e.g.; instant disclosure at Fig. 5A

9. "generating matched information with an integrated circuit digital signal processor in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information" (e.g. claim 63). *See* e.g.:

> A correlation algorithm may be described as searching a trace signal in the temporal-domain or phase-domain to find a match with a pilot signal, wherein the correlation computation is extremely sensitive to phase considerations and may have only a secondary sensitivity to amplitude considerations. *See* instant disclosure 55:15-18 (emphasis added).
>
> A flow diagram is provided in FIG. 5A illustrating the operation of a correlation algorithm in accordance with the present invention. This algorithm may be implemented in a software form with a general purpose digital computer or in a hardwired logic form with a special purpose logical arrangement. For simplicity of discussion, the implementation of the flow diagram set forth in FIG. 5A will be exemplified with a software embodiment using a stored program computer. *See* instant disclosure 105:1-7 (emphasis added). *See* also, e.g.; instant disclosure at Fig. 5A

10. "an integrated circuit synchronization circuit generating a synchronization information" (e.g. claim 67). *See* e.g.:

The correlation program may be synchronized with the input trace signal, where synchronization may be performed with a sync pulse tested in operation 512. If a sync pulse is not detected, the program may loop back around test 512 as a delay until a sync pulse is detected. When a sync pulse is detected in operation 512, the program will branch to outer loop routine 501 to process the trace signal samples. *See* instant disclosure 112:11-16 (emphasis added). *See* also, e.g.; instant disclosure at Fig. 5A
512

11. "an integrated circuit multiple loop iterative processing circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and iteratively generating filtered operands" (e.g. claim 69). *See* e.g.:

Memory devices such as P-store 610 and Z-store 614 may be implemented with a read only memory (ROM) for P-store 610 and with a random access memory (RAM) for Z-store 614 to exemplify use of these different memories devices, as will be discussed in detail with reference to FIG. 6D *See* instant disclosure 139:16-19 (emphasis added). *See* also, e.g.; instant disclosure at Fig. 6D-610

The flow diagram set forth in FIG. 5A represents a real-time correlation algorithm for a plurality of input trace signals processed in a time-shared manner. A plurality of iterative loops are provided to process each sample for each trace signal, which will now be briefly described and which is described in detail hereinafter. *See* instant disclosure 106:19-23 (emphasis added). *See* also, e.g.; instant disclosure at Fig. 5A

12. "a refresh circuit coupled to the integrated circuit dynamic random access alterable memory and refreshing the integrated circuit dynamic random access alterable memory" (e.g. claim 76). *See* e.g.:

For example, refresh circuitry 996 may be implemented with a wellknown automatic gain control (AGC) circuitry. An AGC circuit may operate from the reference signal 962 that is sampled in response to decoder signal 990 asdescribed above. In an alternate embodiment which finds primary advantage in adigital memory arrangement, refresh circuitry 996 may integrate the signals fromCCD memory 932 to provide a gain control signal related to the average of theinformation stored in memory 932. Information in memory 932 may include controlsignals to equalize the number "1"and "0"counts being loaded into memory 932 sothat the integral of the output signals 936 will have an average value of zeroand will have an amplitude related to the degraded signal amplitude. Further,for a digital memory arrangement, refresh circuitry 996 may merely sampledigital one-bits shifted out of CCD memory 932, being indicative of signaldegradation without the use of the reference signal discussed above. . *See* instant

disclosure 392:2-14 (emphasis added). *See* also, e.g.; instant disclosure at Fig. 9F-996,932

13. " a loop heading circuit", "a loop initializing circuit", "a loop looping circuit", "a skipping circuit", "a loop update circuit", "a first output circuit generating product information in response to the input information and in response to the updated loop information", "a second output circuit generating output rounded off product information in response to the product information" and "a loop exiting circuit" (e.g. claim 99). *See* e.g.:

The flow diagram set forth in FIG. 5A represents a real-time correlation algorithm for a plurality of input trace signals processed in a time-shared manner. A plurality of iterative loops are provided to process each sample for each trace signal, which will now be briefly described and which is described in detail hereinafter. *See* instant disclosure 106:19-23 (emphasis added). *See* also, e.g.; instant disclosure at Fig. 5A,5B

14. "an outer loop header circuit", "an outer loop initializing circuit", "an outer loop looping circuit", "an outer loop update circuit", "a middle loop header circuit", "a middle loop initializing circuit", "a middle loop looping circuit", "a middle loop update circuit", "an inner loop header circuit", "an inner loop initializing circuit", "an inner loop looping circuit", "a skipping circuit", "an inner loop update circuit", "a first output circuit generating updated inner loop information in response to the looping through the inner loop", and "a second output circuit generating output rounded off change information in response to the change information" (e.g. claim 104). *See* e.g.:

The flow diagram set forth in FIG. 5A represents a real-time correlation algorithm for a plurality of input trace signals processed in a time-shared manner. A plurality of iterative loops are provided to process each sample for each trace signal, which will now be briefly described and which is described in detail hereinafter. *See* instant disclosure 106:19-23 (emphasis added). *See* also, e.g.; instant disclosure at Fig. 5A,5B

15. "generating radar image information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information" (e.g. claim 107). *See* e.g.:

For example, use of digital filters may significantly enhance processing such as in the medical diagnostic systems, equipment diagonstic systems, radar and sonar signal processing systems, pattern recognition systems, communication systems, and in many other signal processing and data

processing applications. . *See* instant disclosure 4:11-15 (emphasis added). The present invention provides signal processing and digital filtering arrangements for signal enhancement which are applicable to multitudes of different types of systems. In a geophysical exploration system, an improved digital filtering arrangement is provided which yields improved digital filtering capability with a significant reduction in cost when compared to priorart systems. Further, the availability of the low cost and high performance correlator of the present invention permits use of correlation digital filtersin multitudes of applications that previously could not qualify such digital filtering capability. For example, use of digital filters may significantly enhance processing such as in the medical diagnostic systems, equipment diagonstic systems, radar and sonar signal processing systems, patternre cognition systems, communication systems, and in many other signal processing and data processing applications." *See* instant disclosure 4:3-15 (emphasis added). *See* also, e.g.; instant disclosure at Fig. 1

16. "generating medical information with an integrated circuit digital signal processor in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information" (e.g. claim 108).). *See* e.g.:

For example, use of digital filters may significantly enhance processing such as in the medical diagnostic systems, equipment diagonstic systems, radar and sonar signal processing systems, pattern recognition systems, communication systems, and in many other signal processing and data processing applications. . *See* instant disclosure 4:11-15 (emphasis added).

For example, use of digital filters may significantly enhance processing such as in the medical diagnostic systems, equipment diagonstic systems, radar and sonar signal processing systems, pattern recognition systems, communication systems, and in many other signal processing and data processing applications. . *See* instant disclosure 4:11-15 (emphasis added). The present invention provides signal processing and digital filtering arrangements for signal enhancement which are applicable to multitudes of different types of systems. In a geophysical exploration system, an improved digital filtering arrangement is provided which yields improved digital filtering capability with a significant reduction in cost when compared to priorart systems. Further, the availability of the low cost and high performance correlator of the present invention permits use of correlation digital filtersin multitudes of applications that previously could not qualify such digital filtering capability. For example, use of digital filters may significantly enhance processing such as in the medical diagnostic systems, equipment diagonstic systems, radar and sonar signal processing systems, patternre cognition systems, communication systems, and in many other signal processing and data processing applications." *See*

instant disclosure 4:3-15 (emphasis added). *See* also, e.g.; instant disclosure at Fig. 1

17. "an integrated circuit interrupt execution circuit coupled to the integrated circuit instruction execution circuit and coupled to the integrated circuit interrupt input circuit, the integrated circuit interrupt execution circuit interrupting the generating of the first processed information by the integrated circuit instruction execution circuit in response to the input interrupt information generated by the integrated circuit interrupt input circuit" (e.g. claim 109).). *See* e.g.:

1. Factored Data Processing System For Dedicated Applications Ser. No. 101,881 filed on Dec. 28, 1970 by Gilbert P. Hyatt; See instant disclosure 2:25-2 26(emphasis added)

1. Factored Data Processing System For Dedicated Applications Ser. No. 101,881 filed on Dec. 28, 1970 by Gilbert P. Hyatt; *See* instant disclosure 2:25-2 26(emphasis added).

Interrupts

Interrupts may be added virtually without limit. All interrupts are logically ORed together (X5) to transfer operation of the data processor 12 to an interrupt subroutine starting in memory location 04016. The return address is preserved in SPM-2. The interrupt subroutine will scan the discrete interrupt inputs and operate on each interrupt. The interrupt enable (L3) will automatically disable interrupts within interrupts, but may be set with a DO-0 after the return address is SPM-2 has been stored elsewhere under program control, thereby permitting interrupts within interrupts. The end of the interrupt subroutine requires the transfer to the return address, the setting of the interrupt enable (L3) if required, and the transfer indirect (TI) to the return address contained in SPM-2. The interrupt enable (L3) may be used to preserve the contents of SPM-2 against the contingency of an interrupt to permit time shared use of SPM-2.*See* 881 disclosure page 64:8-26(emphasis added).

18. "generating seismic information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information" (e.g. claim 112). *See* e.g.:

Geophysical exploration equipment is primarily used to locate oil, where seismic vibrations are impressed on the earth and geophone transducers sense the reflected seismic signals as indicative of subsurface structures. The received waveforms are extremely complex, including signals from millions of subsurface reflectors all superimposed together with varying amplitudes and with high

levels of noise. The processing of these extremely complex seismic signals is usually performed on large scale computers at computer centers implementing complex filtering computations in software. ." *See* instant disclosure 13:4-11 (emphasis added

For example, use of digital filters may significantly enhance processing such as in the medical diagnostic systems, equipment diagonstic systems, radar and sonar signal processing systems, pattern recognition systems, communication systems, and in many other signal processing and data processing applications. . *See* instant disclosure 4:11-15 (emphasis added). The present invention provides signal processing and digital filtering arrangements for signal enhancement which are applicable to multitudes of different types of systems. In a geophysical exploration system, an improved digital filtering arrangement is provided which yields improved digital filtering capability with a significant reduction in cost when compared to priorart systems. Further, the availability of the low cost and high performance correlator of the present invention permits use of correlation digital filtersin multitudes of applications that previously could not qualify such digital filtering capability. For example, use of digital filters may significantly enhance processing such as in the medical diagnostic systems, equipment diagonstic systems, radar and sonar signal processing systems, patternre cognition systems, communication systems, and in many other signal processing and data processing applications." *See* instant disclosure 4:3-15 (emphasis added). *See* also, e.g.; instant disclosure at Fig. 1

19. "an integrated circuit indexing circuit coupled to the integrated circuit read only memory address circuit and coupled to the integrated circuit index memory, the integrated circuit indexing circuit generating an indexed instruction address in response to the index operand stored in the index memory and in response to at least one of the instruction addresses generated by the integrated circuit read only memory address circuit" (e.g. claim 115). *See* e.g.:

1. Factored Data Processing System For Dedicated Applications Ser. No. 101,881 filed on Dec. 28, 1970 by Gilbert P. Hyatt; See instant disclosure 2:25-2 26(emphasis added)

15. TI (transfer indirect) 0110-0111
This is a one-byte indexable instruction having the above operation code. It causes the address of the next instruction to be obtained from SPM-2 and the return address stored in SPM-2. It goes through micro-operations FA, FY and FZ. *See* 881 disclosure page 74:6-11(emphasis added).

20. "the integrated circuit read only memory accessing circuit further coupled to the integrated circuit indirect transfer memory and generating an accessed indirectly transferred computer instruction in response to at least one of the computer instructions stored in the integrated circuit read only memory, in response to the indirect transfer address stored in the integrated circuit indirect transfer memory, and in response to the indirect transfer information generated by the integrated circuit indirect transfer circuit" (e.g. claim 115). *See* e.g.:

> 1. Factored Data Processing System For Dedicated Applications Ser. No. 101,881 filed on Dec. 28, 1970 by Gilbert P. Hyatt; See instant disclosure 2:25-2 26(emphasis added)
>
> 15. TI (transfer indirect) 0110-0111
> This is a one-byte indexable instruction having the above operation code. It causes the address of the next instruction to be obtained from SPM-2 and the return address stored in SPM-2. It goes through micro-operations FA, FY and FZ. *See* 881 disclosure page 74:6-11(emphasis added).
>
> A general purpose data processor is provided which is fully implementable with integrated circuits. Thus, an integrated circuit in read-only memory (ROM) provides an example of a capability not found in present data processing systems. Other examples are a random access memory (RAM) and other types of flip flop memories used alone or in combinations of integrated circuit memories for this data processing system. *See* 881 disclosure page 6:7-13(emphasis added).

21. "an integrated circuit read only memory accessing circuit generating an accessed directly transferred computer instruction in response to at least one of the computer instructions stored in the integrated circuit read only memory and in response to the direct transfer information generated by the integrated circuit direct transfer circuit" (e.g. claim 119). *See* e.g.:

> 1. Factored Data Processing System For Dedicated Applications Ser. No. 101,881 filed on Dec. 28, 1970 by Gilbert P. Hyatt; See instant disclosure 2:25-2 26(emphasis added)
>
> A general purpose data processor is provided which is fully implementable with integrated circuits. Thus, an integrated circuit in read-only memory (ROM) provides an example of a capability not found in present data processing systems. Other examples are a random access memory (RAM) and other types of flip flop memories used alone or in combinations of

integrated circuit memories for this data processing system. *See* 881 disclosure page 6:7-13(emphasis added).

4. TR (unconditional transfer) 0010-0111.

This is a three-byte instruction in which the above operation code is contained in the first byte and an operand address defined by the second and third bytes. This instruction will cause the next instruction to be accessed from the transfer address location defined by the second and third bytes. The return address is preserved in SPM-2. This instruction goes through micro-operations FA, FL, FM, FN, FO, FP, FQ, FJ, FY and FZ. *See* 881 disclosure page 70:9-17 (emphasis added).

22. "generating processed information with an integrated circuit digital signal processor having an indirect transfer instruction" (e.g. claim 122). *See* e.g.:

1. Factored Data Processing System For Dedicated Applications Ser. No. 101,881 filed on Dec. 28, 1970 by Gilbert P. Hyatt; See instant disclosure 2:25-2 26(emphasis added)

15. TI (transfer indirect) 0110-0111

This is a one-byte indexable instruction having the above operation code. It causes the address of the next instruction to be obtained from SPM-2 and the return address stored in SPM-2. It goes through micro-operations FA, FY and FZ. *See* 881 disclosure page 74:6-11(emphasis added).

A general purpose data processor is provided which is fully implementable with integrated circuits. Thus, an integrated circuit in read-only memory (ROM) provides an example of a capability not found in present data processing systems. Other examples are a random access memory (RAM) and other types of flip flop memories used alone or in combinations of integrated circuit memories for this data processing system. *See* 881 disclosure page 6:7-13(emphasis added).

23. "generating processed information with an integrated circuit digital signal processor having an index instruction" (e.g. claim 124). *See* e.g.:

1. Factored Data Processing System For Dedicated Applications Ser. No. 101,881 filed on Dec. 28, 1970 by Gilbert P. Hyatt; See instant disclosure 2:25-2 26(emphasis added)

16. IS (index) 0110-1I2I1I0

This is a one-byte indexable functional modifier having the operation code contained in the five most significant bits and an address defining an

SPM-Register containing an operand contained in the three least significant bits. A first index (IP or IS) instruction following a second index (IP or IS) instruction will cause the operand address of the second index (IP or IS) instruction to be indexed by the operand of the first index (IP or IS) instruction. Multilevel indexing is thus permissible without limit. Only SPM-Registers 0 through 7 may be used as index registers. This is a single byte functional modifier programmed immediately prior to an instruction to be indexed. This instruction goes through micro-operations FA, FV and FZ. 6 *See* instant disclosure 74:8-16 (emphasis added).

24. "A digital signal processor comprising:... an integrated circuit interrupt execution circuit... an integrated circuit indexing circuit...an integrated circuit direct transfer circuit... an integrated circuit indirect transfer circuit... an integrated circuit instruction execution circuit" (e.g. claim 125). *See* e.g.:

1. Factored Data Processing System For Dedicated Applications Ser. No. 101,881 filed on Dec. 28, 1970 by Gilbert P. Hyatt; See instant disclosure 2:25-2 26(emphasis added)

Interrupts
Interrupts may be added virtually without limit. All interrupts are logically ORed together (X5) to transfer operation of the data processor 12 to an interrupt subroutine starting in memory location 04016. The return address is preserved in SPM-2. The interrupt subroutine will scan the discrete interrupt inputs and operate on each interrupt. The interrupt enable (L3) will automatically disable interrupts within interrupts, but may be set with a DO-0 after the return address is SPM-2 has been stored elsewhere under program control, thereby permitting interrupts within interrupts. The end of the interrupt subroutine requires the transfer to the return address, the setting of the interrupt enable (L3) if required, and the transfer indirect (TI) to the return address contained in SPM-2. The interrupt enable (L3) may be used to preserve the contents of SPM-2 against the contingency of an interrupt to permit time shared use of SPM-2.*See* 881 disclosure page 64:8-26(emphasis added).

A general purpose data processor is provided which is fully implementable with integrated circuits. Thus, an integrated circuit in read-only memory (ROM) provides an example of a capability not found in present data processing systems. Other examples are a random access memory (RAM) and other types of flip flop memories used alone or in combinations of integrated circuit memories for this data processing system. *See* 881 disclosure page 6:7-13(emphasis added).

25. "a frame loop header circuit", "a frame loop initializing circuit", "a frame loop looping circuit", "a frame loop update circuit", "a block loop header circuit", "a block loop initializing circuit", "a block loop looping circuit", "a block loop update circuit", "a sample loop header circuit", "a sample loop initializing circuit", "a sample loop looping circuit", "a skipping circuit", "a sample loop update circuit", "a first output circuit generating product information in response to the input information and in response to the updated sample loop information", and "a second output circuit generating output rounded off product information in response to the product information" (e.g. claim 134). *See* e.g.:

> The flow diagram set forth in FIG. 5A represents a real-time correlation algorithm for a plurality of input trace signals processed in a time-shared manner. A plurality of iterative loops are provided to process each sample for each trace signal, which will now be briefly described and which is described in detail hereinafter. *See* instant disclosure 106:19-23 (emphasis added). *See* also, e.g.; instant disclosure at Fig. 5A,5B, *See* instant disclosure 103-109 for loop discussion

26. "a communication circuit coupled to the integrated circuit instruction execution circuit and communicating information to a remote location in response to the processed information generated by the integrated circuit instruction execution unit" (e.g. claim 136). *See* e.g.:

> Many other output devices are well known in the art and may be used with the system of the present invention, where output device 118 may even be a data communications terminal for communicating information with a remote computer center over telephone lines or over a microwave data link. Therefore, output device 118 is considered to be a generalized output device that may be satisfied by any user system, data acquisition system, data communication system, or other such arrangements. . *See* instant disclosure 172:4-10 (emphasis added). *See* also, e.g.; instant disclosure at Fig. 1A-118,

27. "generating processed information with an integrated circuit digital signal processor having a read only memory write instruction" (e.g. claim 140). *See* e.g.:

> 1. Factored Data Processing System For Dedicated Applications Ser. No. 101,881 filed on Dec. 28, 1970 by Gilbert P. Hyatt; See instant disclosure 2:25-2 26(emphasis added)

A general purpose data processor is provided which is fully implementable with integrated circuits. Thus, an integrated circuit in read-only memory (ROM) provides an example of a capability not found in present data processing systems. Other examples are a random access memory (RAM) and other types of flip flop memories used alone or in combinations of integrated circuit memories for this data processing system. *See* 881 disclosure page 6:7-13(emphasis added). 68:13-69:5

2. ST (store (A) in CM) 0010-0101.

This is a one byte instruction having the above operation code. It causes a two-byte operand previously stored in the A-Register to be stored in a memory location whose address is stored in the 12 least significant bits of the SPM-2 register. The first byte (lsh) of the operand is loaded into the memory location addressed by SPM-2 and the second byte (msh) of the operand is loaded into the memory location following the first byte. The operand is also preserved in A. The operand address is incremented twice, identifying the memory location following the second byte, and returned to SPM-2 where it is preserved. This permits a second operand to be loaded into the A-Register and then transferred to the next-in-line memory location with a second ST instruction. The next instruction address is also preserved and can be used to access the next instruction. The micro-operations used during this instruction are FA, FD, FE, FG, FF, FH, FI, FJ, FY, and FZ. . *See* 881 disclosure page 68:13-69:5(emphasis added).

Adaptive Memory Control

The data processor 12 incorporates an adaptive memory control that adds additional memory protection to insure that the power turn-on condition does not cause detrimental system operation and provide protection from loss of program. In the data processor, this power condition is detected and used to initiate a power interrupt (L1Q); which forces the data processor to look at a specific memory address (040 HEXADECIMAL) by preloading this address into the M-Register. The data processor will continue to access this address until the power interrupt condition is alleviated. In prior art systems, the power interrupt is eliminated when the voltages come within tolerance. In this invention, adaptive techniques are used that insures that not only are the voltages back into tolerance levels, but memory can be properly accessed. This technique is implemented with a memory access interlock implemented by requiring that an instruction that generates a discrete output (DO-2) be located in the first location of the power interrupt program in memory. This discrete output (DO-2) instruction provides the adaptive interlock to insure that memory cannot be accessed before the power interrupt is exited. *See* 881 disclosure page 65:6-20 (emphasis added).

28. generating processed information with an integrated circuit digital signal processor having a decrement instruction" (e.g. claim 142). *See* e.g.:

1. Factored Data Processing System For Dedicated Applications Ser. No. 101,881 filed on Dec. 28, 1970 by Gilbert P. Hyatt; See instant disclosure 2:25-2 26(emphasis added)

A general purpose data processor is provided which is fully implementable with integrated circuits. Thus, an integrated circuit in read-only memory (ROM) provides an example of a capability not found in present data processing systems. Other examples are a random access memory (RAM) and other types of flip flop memories used alone or in combinations of integrated circuit memories for this data processing system. *See* 881 disclosure page 6:7-13(emphasis added). 68:13-69:5

9. BP (subtract) 0011-I3I2I1I0

This is a one-byte indexable instruction wherein the operation code is contained within the first four bits and an operand address is identified by the second four bits. It causes an operand stored in an SPM-Register defined by the operand address to be subtracted from the contents of the A-Register and the results stored in the A-Register. This instruction goes through micro-operations FA, FK, FM, FN, FO, FP, FQ, FR, FU, and FZ*See* also '881 page 69:6-12 TX instruction

29. "generating processed information with an integrated circuit digital signal processor haying a decrement and transfer instruction" (e.g. claim 144). *See* e.g.:

1. Factored Data Processing System For Dedicated Applications Ser. No. 101,881 filed on Dec. 28, 1970 by Gilbert P. Hyatt; See instant disclosure 2:25-2 26(emphasis added)

3. TX (decrement and transfer on non-negative) 0010-0110.
This may be either a three or a four-byte and defines an index register. The absence of an index byte defines the SPM- 0 Register. The second byte contains the above operation code and the third and fourth bytes define an operand address. A non- negative decremented number will cause the next instruction to be accessed from the transfer address location defined by the last two bytes of this instruction. The return address is stored in the SPM-2 Register. A negative decremented number will cause the next instruction to be accessed from the byte following the last byte (address byte 2). The transfer address (which is not used) is preserved in SPM-2.This instruction is used to guide the data processor through a loop one or more times. The desired number of transfers, less one, is initially loaded into the appropriate index register. This number will then be decremented through zero to a negative number before the loop is exited.As long as the decremented

number is non-negative, the TX instruction goes through micro-operations FC, FL, FM, Fn, FO, FP, FQ, FJ, FY, and FZ.

As soon as the decremented number becomes negative, the TX instruction goes through micro-operations FC, FAI, and FZ. *See* also '881 page 69:6-70:6

30. "generating processed information with an integrated circuit digital signal processor having a conditional transfer instruction" (e.g. claim 146). *See* e.g.:

1. Factored Data Processing System For Dedicated Applications Ser. No. 101,881 filed on Dec. 28, 1970 by Gilbert P. Hyatt; See instant disclosure 2:25-2 26(emphasis added)

3. TX (decrement and transfer on non-negative) 0010-0110.
This may be either a three or a four-byte and defines an index register. The absence of an index byte defines the SPM- 0 Register. The second byte contains the above operation code and the third and fourth bytes define an operand address. A non- negative decremented number will cause the next instruction to be accessed from the transfer address location defined by the last two bytes of this instruction. The return address is stored in the SPM-2 Register. A negative decremented number will cause the next instruction to be accessed from the byte following the last byte (address byte 2). The transfer address (which is not used) is preserved in SPM-2.This instruction is used to guide the data processor through a loop one or more times. The desired number of transfers, less one, is initially loaded into the appropriate index register. This number will then be decremented through zero to a negative number before the loop is exited.As long as the decremented number is non-negative, the TX instruction goes through micro-operations FC, FL, FM, Fn, FO, FP, FQ, FJ, FY, and FZ.

As soon as the decremented number becomes negative, the TX instruction goes through micro-operations FC, FAI, and FZ. *See* also '881 page 69:6-70:6

A general purpose data processor is provided which is fully implementable with integrated circuits. Thus, an integrated circuit in read-only memory (ROM) provides an example of a capability not found in present data processing systems. Other examples are a random access memory (RAM) and other types of flip flop memories used alone or in combinations of integrated circuit memories for this data processing system. *See* 881 disclosure page 6:7-13(emphasis added). 68:13-69:5

31. "generating processed information with an integrated circuit digital signal processor having a skip on condition instruction" (e.g. claim 156). *See* e.g.:

1. Factored Data Processing System For Dedicated Applications Ser. No. 101,881 filed on Dec. 28, 1970 by Gilbert P. Hyatt; See instant disclosure 2:25-2 26(emphasis added)

A general purpose data processor is provided which is fully implementable with integrated circuits. Thus, an integrated circuit in read-only memory (ROM) provides an example of a capability not found in present data processing systems. Other examples are a random access memory (RAM) and other types of flip flop memories used alone or in combinations of integrated circuit memories for this data processing system. *See* 881 disclosure page 6:7-13(emphasis added).

. Factored Data Processing System For Dedicated Applications Ser. No. 101,881 filed on Dec. 28, 1970 by Gilbert P. Hyatt; See instant disclosure 2:25-2 26(emphasis added)

29. SK (skip on discrete) 111I4-I3I2I1I0

This is a one-byte indexable instruction wherein the three most significant bits identify the operation code and the five least significant bits identify a discrete input channel address. If a discrete exists on the addressed channel, three bytes (usually a transfer instruction) are skipped and the next instruction is obtained from the fourth byte following the skip on discrete instruction. If a discrete does not exist on the addressed channel, the next instruction (usually a three-byte transfer instruction) is obtained from the three bytes immediately following the skip on discrete instruction. This instruction goes through micro-operations FA, FAC and FZ. . *See* 881 disclosure pages 78:18-79:6 (emphasis added).

32. "generating processed information with an integrated circuit digital signal processor having a serial input instruction" (e.g. claim 157). *See* e.g.:

.1 Factored Data Processing System For Dedicated Applications Ser. No. 101,881 filed on Dec. 28, 1970 by Gilbert P. Hyatt; See instant disclosure 2:25-2 26(emphasis added)

A general purpose data processor is provided which is fully implementable with integrated circuits. Thus, an integrated circuit in read-only memory (ROM) provides an example of a capability not found in present data processing systems. Other examples are a random access memory (RAM) and other types of flip flop memories used alone or in combinations of integrated circuit memories for this data processing system. *See* 881 disclosure page 6:7-13(emphasis added).

25. EX (input/output word) 1010-I3I2I1I0

This is a one-byte indexable instruction wherein the four most significant bits identify the operation code and the four least significant bits identify an I/O channel address. The contents of the A-Register are output to the addressed channel while the contents of the addressed channel are simultaneously loaded into the A-Register. A shift enable signal is output to gate 16 clock pulses to the selected channel. This instruction goes through micro-operations FA, FAB, and FZ. . *See* 881 disclosure page 77:14-78:2(emphasis added).

33. "generating processed information with an integrated circuit digital signal processor having a discrete output instruction" (e.g. claim 159). *See* e.g.:

1. Factored Data Processing System For Dedicated Applications Ser. No. 101,881 filed on Dec. 28, 1970 by Gilbert P. Hyatt; See instant disclosure 2:25-2 26(emphasis added)

A general purpose data processor is provided which is fully implementable with integrated circuits. Thus, an integrated circuit in read-only memory (ROM) provides an example of a capability not found in present data processing systems. Other examples are a random access memory (RAM) and other types of flip flop memories used alone or in combinations of integrated circuit memories for this data processing system. *See* 881 disclosure page 6:7-13(emphasis added).

25. EX (input/output word) 1010-I3I2I1I0

This is a one-byte indexable instruction wherein the four most significant bits identify the operation code and the four least significant bits identify an I/O channel address. The contents of the A-Register are output to the addressed channel while the contents of the addressed channel are simultaneously loaded into the A-Register. A shift enable signal is output to gate 16 clock pulses to the selected channel. This instruction goes through micro-operations FA, FAB, and FZ. . *See* 881 disclosure page 77:14-78:2(emphasis added).

34. "generating processed information with an integrated circuit digital signal processor having a discrete output instruction" (e.g. claim 159). *See* e.g.:

1. Factored Data Processing System For Dedicated Applications Ser. No. 101,881 filed on Dec. 28, 1970 by Gilbert P. Hyatt; See instant disclosure 2:25-2 26(emphasis added)

A general purpose data processor is provided which is fully implementable with integrated circuits. Thus, an integrated circuit in read-only memory (ROM) provides an example of a capability not found in present data processing systems. Other examples are a random access memory (RAM) and other types of flip flop memories used alone or in combinations of integrated circuit memories for this data processing system. *See* 881 disclosure page 6:7-13(emphasis added).

Discrete Outputs
The data processor 12 can generate discrete outputs (DO) to meet specific requirements under program control. The DO assignments are:
DO-0 Spare
DO-1 Provide clock pulses to ASR-33 (teletypewriter).
DO-2 Provides a clock to set the power turn-on interrupt, L1. A DO-2 instruction (1100-0010) will be contained in program memory location 4016 to reset L1 during power turn- on.
DO-3 Iteration timer reset (not implemented).
DO-4 Trigger to I2 latch, the discrete input-4 (DI-4) input. The I2 flip-flop is automatically zero set during the power on sequence.
DO-5 Trigger to I3 latch, the discrete input-5 (DI-5) input. The I3 flip-flop is automatically zero set during the power turn-on sequence.

DO-6 Trigger to the I4 latch, the discrete input-6 (DI- 6) input. The I4 flip-flop is automatically zero set during the power turn-on sequence.
DO-7 Intensity control (2 line)(not implemented).
DO-8 Toggles the I1 flip-flop causing scratch pad memory paging.
DO-9 Core memory paging.
DO-10 Not implemented.
DO-11
See 881 disclosure page 6216-63:14(emphasis added).

35. "generating processed information with an integrated circuit digital signal processor having a skip on discrete instruction" (e.g. claim 166). *See* e.g.:

1. Factored Data Processing System For Dedicated Applications Ser. No. 101,881 filed on Dec. 28, 1970 by Gilbert P. Hyatt; See instant disclosure 2:25-2 26(emphasis added)

A general purpose data processor is provided which is fully implementable with integrated circuits. Thus, an integrated circuit in read-only memory (ROM) provides an example of a capability not found in present data processing systems. Other examples are a random access memory (RAM) and other types of flip flop memories used alone or in combinations of integrated circuit memories for this data processing system. *See* 881 disclosure page 6:7-13(emphasis added).

29. SK (skip on discrete) 111I4-I3I2I1I0
This is a one-byte indexable instruction wherein the three most significant bits identify the operation code and the five least significant bits identify a discrete input channel address. If a discrete exists on the addressed channel, three bytes (usually a transfer instruction) are skipped and the next instruction is obtained from the fourth byte following the skip on discrete instruction. If a discrete does not exist on the addressed channel, the next instruction (usually a three-byte transfer instruction) is obtained from the three bytes immediately following the skip on discrete instruction. This instruction goes through micro-operations FA, FAC and FZ. . *See* 881 disclosure page 78:18-79:6(emphasis added).

36. "generating processed information with an integrated circuit digital signal processor having power turn on interrupt instruction" (e.g. claim 168). *See* e.g.:

1. Factored Data Processing System For Dedicated Applications Ser. No. 101,881 filed on Dec. 28, 1970 by Gilbert P. Hyatt; See instant disclosure 2:25-2 26(emphasis added)

A general purpose data processor is provided which is fully implementable with integrated circuits. Thus, an integrated circuit in read-only memory (ROM) provides an example of a capability not found in present data processing systems. Other examples are a random

access memory (RAM) and other types of flip flop memories used alone or in combinations of integrated circuit memories for this data processing system. *See* 881 disclosure page 6:7-13(emphasis added).

During the execution of a program instruction, the central processor begins at point 1 at the top center of Fig. 5. The first branch condition is Y3 - C3Q.C2Q.C1Q.C0Q.K11Q.K10Q.I1.I0+K2Q.
If this term is true, the FC micro-operation is performed; if not true, a second control condition is tested. If flip-flop K1 is in the 0 state, the FA micro-operation is executed and if it is in the 1 state, the FB micro-operation is executed. In similar fashion, a series of micro-operations are executed in accordance with the programmed instruction until the micro-operation FZ is completed. At this point the power- interrupt flip-flop L1 determines whether or not the execution of programmed instructions continues. If the L1 flip-flop is in the 1 state indicating an interrupt, a series of micro-operations is entered which place the return address in SPM2 and loads the interrupt routine address into the M-register. If the L1 flip- flop is in the 0 state indicating a non-interrupt condition, the processor returns to point 1 and begins the execution of another program instruction unless an X5 signal indicates that there is an external interrupt. If there is an external interrupt, the data processor ignores it, returning to point 1 unless the interrupt override flip-flop L3 is true and the flip-flop K1 is in the false state. . *See* 881 disclosure page 39:19-40:12(emphasis added).

37. "a machine data processor implemented on a single integrated circuit chip" (e.g. claim 171). *See* e.g.:

1. Factored Data Processing System For Dedicated Applications Ser. No. 101,881 filed on Dec. 28, 1970 by Gilbert P. Hyatt; See instant disclosure 2:25-2 26(emphasis added)

A general purpose data processor is provided which is fully implementable with integrated circuits. Thus, an integrated circuit in read-only memory (ROM) provides an example of a capability not found in present data processing systems. Other examples are a random access memory (RAM) and other types of flip flop memories used alone or in combinations of integrated circuit memories for this data processing system. *See* 881 disclosure page 6:7-13(emphasis added).

38. "a data processor implemented on a single integrated circuit chip" (e.g. claim 172).

1. Factored Data Processing System For Dedicated Applications Ser. No. 101,881 filed on Dec. 28, 1970 by Gilbert P. Hyatt; See instant disclosure 2:25-2 26(emphasis added)

A general purpose data processor is provided which is fully implementable with integrated circuits. Thus, an integrated circuit in read-only memory (ROM) provides an example of a capability not found in present data processing systems. Other examples are a random access memory (RAM) and other types of flip flop memories used alone or in combinations of integrated circuit memories for this data processing system. *See* 881 disclosure page 6:7-13(emphasis added).

39. "a photo optical machine coupled to the data processor implemented on the single integrated circuit chip, the photo optical machine generating a photo optical mask in response to data processed by the data processor" (e.g. claim 174).

1. Factored Data Processing System For Dedicated Applications Ser. No. 101,881 filed on Dec. 28, 1970 by Gilbert P. Hyatt; See instant disclosure 2:25-2 26(emphasis added)

A general purpose data processor is provided which is fully implementable with integrated circuits. Thus, an integrated circuit in read-only memory (ROM) provides an example of a capability not found in present data processing systems. Other examples are a random access memory (RAM) and other types of flip flop memories used alone or in combinations of integrated circuit memories for this data processing system. *See* 881 disclosure page 6:7-13(emphasis added).

Detailed Description
Introduction

By way of example, a factored computer system is represented in block diagram form in Fig. 1 as a numerical control system 10, including an electronic data processor 12, arranged in accordance with the invention. The specific example referred to here and described hereafter relates to a three-axis controlled milling machine, but it will readily be appreciated that systems in accordance with the invention may be applied to a wide variety of tasks including communication, process control, processing of business data and other control functions such as photo optical pattern generators and multi-turret machines. *See* 881 disclosure page 9:1-9(emphasis added).

40. "a pattern generator coupled to the data processor implemented on the single integrated circuit chip, the pattern generator machine generating a pattern in response to data processed by the data processor" (e.g. claim 175).

1. Factored Data Processing System For Dedicated Applications Ser. No. 101,881 filed on Dec. 28, 1970 by Gilbert P. Hyatt; See instant disclosure 2:25-2 26(emphasis added)

A general purpose data processor is provided which is fully implementable with integrated circuits. Thus, an integrated circuit in read-only memory (ROM) provides an example of a capability not found in present data processing systems. Other examples are a random access memory (RAM) and other types of flip flop memories used alone or in combinations of integrated circuit memories for this data processing system. *See* 881 disclosure page 6:7-13(emphasis added).

Detailed Description
Introduction

By way of example, a factored computer system is represented in block diagram form in Fig. 1 as a numerical control system 10, including an electronic data processor 12, arranged in accordance with the invention. The specific example referred to here and described hereafter relates to a three-axis controlled milling machine, but it will readily be appreciated that systems in accordance with the invention may be applied to a wide variety of tasks including communication, process control, processing of business data and other control functions such as photo optical pattern generators and multi-turret machines. *See* 881 disclosure page 9:1-9(emphasis added).

41. "a plotter coupled to the data processor implemented on the single integrated circuit chip, the plotter generating a plot in response to data processed by the data processor" (e.g. claim 176).

1. Factored Data Processing System For Dedicated Applications Ser. No. 101,881 filed on Dec. 28, 1970 by Gilbert P. Hyatt; See instant disclosure 2:25-2 26(emphasis added)

A general purpose data processor is provided which is fully implementable with integrated circuits. Thus, an integrated circuit in read-only memory (ROM) provides an example of a capability not found in present data processing systems. Other examples are a random access memory (RAM) and other types of flip flop memories used alone or in combinations of integrated circuit memories for this data processing system. *See* 881 disclosure page 6:7-13(emphasis added).

One technical area in which systems in accordance with the invention have particular advantage is in the control of multi- axis machine tools and the control of photo optical plotters to provide output product. *See* 881 disclosure page 12:18-20(emphasis added).

42. "a read only memory implemented on a single integrated circuit chip; and an alterable memory implemented on the single integrated circuit chip" (e.g. claim 177).

1. Factored Data Processing System For Dedicated Applications Ser. No. 101,881 filed on Dec. 28, 1970 by Gilbert P. Hyatt; See instant disclosure 2:25-2 26(emphasis added)

A general purpose data processor is provided which is fully implementable with integrated circuits. Thus, an integrated circuit in read-only memory (ROM) provides an example of a capability not found in present data processing systems. Other examples are a random access memory (RAM) and other types of flip flop memories used alone or in combinations of integrated circuit memories for this data processing system. *See* 881 disclosure page 6:7-13(emphasis added).

43. "generating processed information with an integrated circuit digital signal processor having save return address microinstruction in response to the digital signal processor program and in response to the input information" (e.g. claim 184).

1. Factored Data Processing System For Dedicated Applications Ser. No. 101,881 filed on Dec. 28, 1970 by Gilbert P. Hyatt; See instant disclosure 2:25-2 26(emphasis added)

A general purpose data processor is provided which is fully implementable with integrated circuits. Thus, an integrated circuit in read-only memory (ROM) provides an example of a capability not found in present data processing systems. Other examples are a random access memory (RAM) and other types of flip flop memories used alone or in combinations of integrated circuit memories for this data processing system. *See* 881 disclosure page 6:7-13(emphasis added).

4. TR (unconditional transfer) 0010-0111.

This is a three-byte instruction in which the above operation code is contained in the first byte and an operand address defined by the second and third bytes. This instruction will cause the next instruction to be accessed from the transfer address location defined by the second and third bytes. The return address is preserved in SPM-2. This instruction goes through micro-operations FA, FL, FM, FN, FO, FP, FQ, FJ, FY and FZ. *See* 881 disclosure page 70:7-12(emphasis added).

44. "making a disk memory product in response to the processed information" (e.g. claim 188).

For example, counter 993 provides operation similar to the bit, word, and sector counters associated with well known prior art disk memories which are used for counting disk memory clock pulses to keep track of the location of information on a rotating disk. *See* instant disclosure 379:9-13 (emphasis added).

The Board addressed the "making a product" claims in the Decision on appeal regarding related copending application Serial No. 08/471,698; Appeal No. 2002-2032: reversing in part rejections of such claims under § 112-1 and § 112-2. See also, e.g.; the following:

.1 Factored Data Processing System For Dedicated Applications Ser. No. 101,881 filed on Dec. 28, 1970 by Gilbert P. Hyatt; See instant disclosure 2:25-2 26(emphasis added)

A general purpose data processor is provided which is fully implementable with integrated circuits. Thus, an integrated circuit in read-only memory (ROM) provides an example of a capability not found in present data processing systems. Other examples are a random access memory (RAM) and other types of flip flop memories used alone or in combinations of integrated circuit memories for this data processing system. *See* 881 disclosure page 6:7-13(emphasis added).

45. "writing digital signal processor operands into the integrated circuit read only memory in response to the digital signal processor program and in response to the input information" (e.g. claim 202).

.1 Factored Data Processing System For Dedicated Applications Ser. No. 101,881 filed on Dec. 28, 1970 by Gilbert P. Hyatt; See instant disclosure 2:25-2 26(emphasis added)

A general purpose data processor is provided which is fully implementable with integrated circuits. Thus, an integrated circuit in read-only memory (ROM) provides an example of a capability not found in present data processing systems. Other examples are a random access memory (RAM) and other types of flip flop memories used alone or in combinations of integrated circuit memories for this data processing system. *See* 881 disclosure page 6:7-13(emphasis added).

As shown in Fig. 12 an A section Scratch Pad Memory printed circuit board includes eight integrated circuit shift registers 234. A binary coded decimal to decimal decoder 236 generates memory select signals P50 through P57 which is gated through a first series of gates 238. This first gated signal in turn gates a clock signal P3A through a second series of gates 240 to clock a selected one of the registers. The outputs from the registers 234 are multiplexed into signals P120A and P121A, each carrying outputs from four of the registers. Three additional scratch pad memory sections B, C and D, identical with A shown in Fig. 12 provide corresponding output signals P120B, 121B, 120C, 121C, 120D and 121D. These in turn are multiplexed by NAND gate 242 into a single output signal P85. The signals in the B, C and D sections correspond to those of the A section and are defined according to terminal numbers as follows: . *See* 881 disclosure page 81:10-20(emphasis added).

46. "making a payroll product in response to the first processed information" (e.g. claim 212).

1. Factored Data Processing System For Dedicated Applications Ser. No. 101,881 filed on Dec. 28, 1970 by Gilbert P. Hyatt; See instant disclosure 2:25-2 26(emphasis added)

The Board addressed the "making a product" claims in the Decision on appeal regarding related copending application Serial No. 08/471,698; Appeal No. 2002-2032: reversing in part rejections of such claims under § 112-1 and § 112-2. See also, e.g.; the following:

> One technical area in which systems in accordance with the invention have particular advantage is in the control of multi- axis machine tools and the control of photo optical plotters to provide output product. Other areas of particular advantage include the processing of communications and business data, for instance, payroll processing and inventory control. *See* 881 disclosure page 12:18-13:2(emphasis added).

47. "making an inventoried product in response to the second processed information" (e.g. claim 218).

> 1. Factored Data Processing System For Dedicated Applications Ser. No. 101,881 filed on Dec. 28, 1970 by Gilbert P. Hyatt; See instant disclosure 2:25-2 26(emphasis added)

The Board addressed the "making a product" claims in the Decision on appeal regarding related copending application Serial No. 08/471,698; Appeal No. 2002-2032: reversing in part rejections of such claims under § 112-1 and § 112-2. See also, e.g.; the following:

> One technical area in which systems in accordance with the invention have particular advantage is in the control of multi- axis machine tools and the control of photo optical plotters to provide output product. Other areas of particular advantage include the processing of communications and business data, for instance, payroll processing and inventory control. *See* 881 disclosure page 12:18-13:2(emphasis added).

48. "making a ~~natural resource~~ product in response to the first processed information" (e.g. claim 225).
[CLAIM 225 HAS BEEN AMENDED]

49. "making a telephone product in response to the first processed information" (e.g. **claim 226)** The Board addressed the "making a product" claims in the Decision on appeal regarding related copending application Serial No. 08/471,698; Appeal No. 2002-2032: reversing in part rejections of such claims under § 112-1 and § 112-2. See also, e.g.; the following:

> "A punched tape reader is one form of input means commonly used as an input device to digital equipment. It should be understood that while the term tape reader may be employed hereinafter, this is for purposes of explanation. The same explanation may be applicable to other input means, comprising, to mention a few, any of the following: punched tape readers, magnetic tape readers, punched card readers, magnetic card readers, general purpose digital computers, differential digital analyzers, stored program digital computers, converters such as synchro to digital or analog to digital, shift registers,

latching registers, business machines, typewriters, calculators, communication lines, radar lines, telephone lines, telegraph lines, memory means such as core memories, disk memories, drum memories, or semiconductor memories, keyboards, switches, digitizers, cathode ray tube displays, sensors, pickoffs and encoders. In addition, though the terms sprocket. sprocket hole and sprocket signal are used herein for purposes of explanation, such terms are not meant to be limited in application to punched tape readers, but refer generally to the reference and reference signal of whatever input means is employed." *See* instant disclosure pages 76:1-22 (emphasis added). *See* also, e.g.; instant disclosure at Fig 1 at 16

50. "making a ~~mineral~~ product in response to the third processed information" (e.g. claim 234).
[CLAIM 234 HAS BEEN AMENDED]

51. "making a ~~moving~~ product in response to the first processed information" (e.g. claim 241).
[CLAIM 241 HAS BEEN AMENDED]

52. "making an oil product in response to the first processed information" (e.g. claim 246).

Geophysical exploration equipment is primarily used to locate oil, where seismic vibrations are impressed on the earth and geophone transducers sense the reflected seismic signals as indicative of subsurface structures. The received waveforms are extremely complex, including signals from millions of subsurface reflectors all superimposed together with varying amplitudes and with high levels of noise. The processing of these extremely complex seismic signals is usually performed on large scale computers at computer centers implementing complex filtering computations in software. *See* instant disclosure 13:4-11 (emphasis added).

53. "making a turret product in response to the first processed information" (e.g. claim 248).

. Factored Data Processing System For Dedicated Applications Ser. No. 101,881 filed on Dec. 28, 1970 by Gilbert P. Hyatt; See instant disclosure 2:25-2 26(emphasis added)

The Board addressed the "making a product" claims in the Decision on appeal regarding related copending application Serial No. 08/471,698; Appeal No. 2002-2032: reversing in part rejections of such claims under § 112-1 and § 112-2. See also, e.g.; the following:

By way of example, a factored computer system is represented in block diagram form in Fig. 1 as a numerical control system 10, including an electronic data processor 12, arranged in accordance with the invention. The specific example referred to here and described hereafter relates to a three-axis controlled milling machine, but it will readily be appreciated that systems in accordance with the invention may be applied to a wide variety of tasks including communication, process control, processing of business data and other control functions such as photo optical pattern generators and multi-turret machines. *See* 881 disclosure page 8:3-10(emphasis added).

54. "making a ~~vehicle~~ product in response to the fourth processed information" (e.g. claim 294).

In still another embodiment, a correlator may monitor a vibration sensor such as on a piece of machinery or an aircraft engine for detection of a particular vibration signature, wherein the vibration signal may be continuously generated for extremely long periods of time such as for hours of time and wherein the pilot signal may have a limited duration such as for only seconds of time having three-orders-of-magnitude (factor-of-1,000) difference in duration between the pilot signal and the trace signal. *See* instant disclosure 343:5-12 (emphasis added